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Research Article

Design and Build of an Electrical Machines' High Speed Measurement System at Low Cost

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The principal objective of this paper is to demonstrate the capability of high speed measurement and acquisition equipment design and build in the laboratory at a very low cost. The presented architecture employees highly integrated market components eliminating thus the complexity of the hardware and software stack. The key element of the proposed system is a Hi-Speed USB to Serial/FIFO development module that is provided with full software and driver support for most popular operating systems. This module takes over every single task needed to get the data from the A/D to the user software gluelessly and transparently, solving this way the most difficult problem in data acquisition systems which is the fast and reliable communication with a host computer. Other ideas tested and included in this document offer Hall Effect measuring solutions using some excellent features and very low cost ICs widely available on the market today.

1. Introduction

Today, every researcher, engineer, student, or specialist professional that works with electrical machines needs to study and understand deeper the machine operation transient phenomena and how those affect the machine itself as well as the neighbouring electrical equipment. During the past two decades using data acquisition cards in combination with commercial and academic software for the machine signals sampling conversion and storage has proven to be a very efficient means for the study of the transient and steady state operation of electrical machines. Almost in every university, enterprise R&D department, or other institutions, a laboratory that studies electrical machines is equipped with data acquisition cards and software for storing, converting, and presenting the sampled signals captured during the electrical machine operation [1–3]. In order to capture machine signals, a fast electronic sampling card is necessary to interface the selected currents and voltages of the real world to a host computer via its simultaneously sampling analog to digital converters. A fast communication port such as Gigabit Ethernet or Hi-Speed Universal Serial Bus with rates up to 480 Mbit/sec is the most convenient highway to transfer real time captured data to the host computer for further processing.

Fast data transfer is crucial when concurrent sampling of several electrical signals with higher harmonic content, sometimes up to 20th order, is the case. Modern microprocessors and fast computer peripherals make it now possible to study voltage and current harmonic content for more signals at the same time and in greater harmonics order depth.

In the general case commercial products are used for the signals sampling and transfer to a Host PC, while implementation for both fast [1, 2] and slow [3] sampling systems can be found in the literature. None of them though combines both fast data rates up to 400 Mbit/sec and easy implementation at a remarkably low cost that would allow a laboratory to reproduce unlimited number of sampling systems for its engineers or students.

Electrical machines and power engineers now are quite familiar with embedded systems programming for signal measurements, processing, and control, but fast data communications with a Host PC via a fast interface such as Universal Serial Bus, involve driver level programming on the host side. This is usually a problem for non-software engineers,

especially when speed optimization should be taken to the limit in order to make a full exploit of the peripheral transfer bandwidth.

In order to overcome this difficulty, engineers are obligated to purchase commercial products consisting of both the data acquisition cards and the necessary dedicated driver software that is executed on the Host PC. This driver transfers the captured data from the sampling card to the Host PC transparently with no need for any user action in this procedure. This sounds great since the job is done without any demands for further user interference. The problem is that these hardware and software sampling systems are not consumer products and therefore their cost is driven to significantly high values. Consequently, although it may be easy for a commercial company to buy some sets for its employees, it is not equally feasible for an academic laboratory to provide adequate sets of cards and software licenses for every student or researcher experimenting with electrical machine measurements.

This work proposes an alternative platform consisting of both software [4] and hardware [5] modules that can be easily built in the laboratory, able to transfer multiple signals of electrical machine measurements to the host PC via a Hi-Speed Universal Serial Bus data rate. The proposed Data Acquisition (DAQ) system involves license and royalty free components that can be found on the market at a very low budget. The manufacturer of the USB transfer module used [3] provides the USB driver and several software sample applications for most popular operating systems and high level programming languages, respectively.

2. Sampling System Architecture Overview

The Architecture of the sampling card can be divided in five discrete cascaded hardware and software layers.

The 1st layer (electrical interface) is attached to the current and voltage signals of the electrical machine converting the real measured amounts into voltages adjusted to be suitable for the CMOS and TTL level A/D converters of the next layer.

The 2nd layer (sampling and digitizing layer) is connected to the 1st layer and reads the analog voltages that correspond to the measured currents and voltages. The voltage signals are sampled and digitized by the MCU analog to digital converters and then they are pushed upstream on the 8-bit parallel FIFO of the next layer.

The 3rd layer (transfer layer) reads the bytes arriving to its 8-bit FIFO and transfers them via USB with a speed up to 400 Mbit/sec to the next layer that is a piece of software (driver) running on the Host PC.

The 4th layer (driver layer) is the software that receives the bulk—so far meaningless data—in a receive buffer on the Host PC and keeps them available for the top 5th layer to consume.

The 5th layer (application layer) pumps the 4th layer's buffers and reconstructs the measurements data into a human friendly format for further presentation and processing (Figure 1).

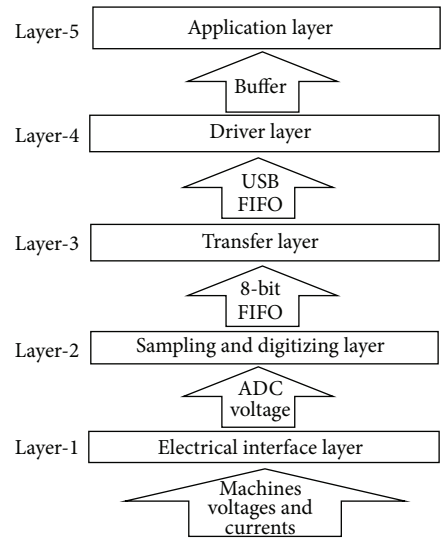

Figure 1: Five layers stack overview of the built electrical machines measurement hardware and software systems.

2.1. Layer 1: Electrical Interface. During transient and steady state study of an electrical machine, the main physical amounts of interest are the various currents and voltages on the machine terminals and on some types of machines the excitation field voltages and currents as well.

Terminal currents in the general case are typically measured after they are galvanically isolated and stepped down by LEM hall effect sensors that are quite expensive and occupy a great deal of space on the printed circuit board. In this work another approach is presented in current measurement by means of using a special Hall Effect sensor IC [6] integrated with a single ceramic package suitable for easy PCB mounting. The IC ACS712 is manufactured by Allegro Microsystems Inc. and is a fully integrated Hall Effect based linear current sensor with 2.1 kV rms voltage isolation and a very low resistance current contactor. The ACS712 device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise proportional voltage is provided by the low offset, chopper stabilized BiCMOS Hall IC, which is programmed for accuracy after packaging. The internal resistance of the conductive path is 1.2 mΩ typical, providing low power loss. Below are stated the main characteristics of the ACS712 AC/DC current measurement IC (Figure 2).

(i) Up to 30 A AC/DC direct measurement.

(ii) Low-noise analog signal path.

(iii) Device bandwidth is set via FILTER pin.

(iv) 50 kHz bandwidth.

(v) Total out err. 1.5% TA = 25°C, 4% at −40°C to 85°C.

(vi) Small footprint, low-profile SOIC8 package.

(vii) 1.2 mΩ internal conductor resistance.

(viii) 2.1 kV RMS minimum isolation voltage.

(ix) 5.0 V, single supply operation.

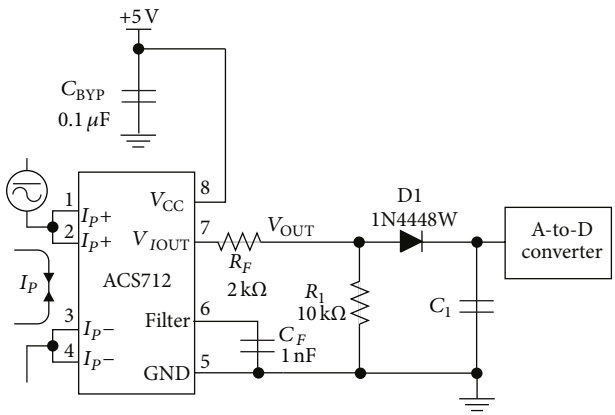

Figure 2: ACS712 outputs an analog signal, VOUT varying linearly with the AC or DC primary sensed current.

(x) 66 to 185 mV/A output sensitivity.

(xi) Output voltage proportional to AC or DC currents.

(xii) Factory-trimmed for accuracy.

(xiii) Extremely stable output offset voltage.

(xiv) Nearly zero magnetic hysteresis.

(xv) Ratiometric output from supply voltage.

The wide bandwidth of the ACS712 chip allows for measurements of 50 ksamples/sec [6] driven to the next layer A/D converter for sampling and digitizing.

If currents lower than 30 A AC/DC are considered for measurement then there is no need for any external part or current transformer to be used as the machine terminal current is driven directly through the ACS712 pins 1-2 and 3-4. The output is a positive voltage signal that contains an offset for zero in order to represent all current variations in the positive variation range of the output voltage.

The Quiescent output voltage is the output of the sensor when the primary current is zero. For a unipolar supply voltage, it nominally remains at $V_{CC}/2$. Thus, V_{CC} = 5 V translates into V_{IOUT}(Q) = 2.5 V. Variation in V_{IOUT}(Q) can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift (Figure 3).

For the voltage measurements a fast optocoupling circuit [7] was designed to offer an interface with basic isolation for the board and the mains voltages. The optocoupler used is the Avago Technologies Inc. HCNR200 (Figure 4).

The HCNR200/201 high-linearity analog optocoupler consists of a high-performance AlGaAs LED that illuminates two closely matched photodiodes. The input photodiode can be used to monitor and, therefore, stabilize the light output of the LED. As a result, the nonlinearity and drift characteristics of the LED can be virtually eliminated. The output photodiode produces a photocurrent that is linearly related to the light output of the LED. The close matching of the photo-diodes and advanced design of the package ensure the high linearity and stable gain characteristics of the optocoupler.

The HCNR200/201 can be used to isolate analog signals in a wide variety of applications that require good stability, linearity, bandwidth, and low cost (Figure 5).

(i) Low nonlinearity: 0.01%.

(ii) Low gain temperature coefficient: −65 ppm/°C.

(iii) Wide bandwidth (DC to >1 MHz).

(iv) Worldwide approval (5 kV rms/1 min, 1414 Vpeak).

2.2. Layer 2: Sampling and Digitizing. After the current and voltage signals are collected and conditioned into appropriate level signals (0–5 VAC), the second layer is responsible for converting the analog signals to digital and to output the data bytes on an 8-bit bus to the transfer layer FIFO.

For the Sampling and Digitizing Layer the designer can use any microcontroller or DSP platform that is already used in other laboratory applications and experiments, provided there are adequate ADC channels with a resolution of at least 10 bits and that the microprocessor is fast enough to perform a sampling rate on the 8 analog channels that exceeds eight times the 50 ksamples/sec of each ACS712 channel which sets the limits for all system sampling speed.

As known, sampling is the process of converting a continuous-time signal $x(t)$ into a discrete time sequence $x[n]$. The $x[n]$ is obtained by extracting $x(t)$ every T seconds where T is the sampling period (Figure 6).

The relationship between $x(t)$ and $x[n]$ is given by (Figure 7)

$$X[n] = x(t)|_{t=nT} = x(nT), \quad n = \ldots, -1, 0, 1, 2, \ldots. \quad (1)$$

The maximum available sampling bandwidth to avoid aliasing is limited from the ACS712 maximum response frequency that is 50 kHz [6]. This corresponds to a sampling microcontroller minimum rate of 100 kHz. In practice we always perform some oversampling to avoid any case of aliasing. In the presented test system built the sampling and digitizing layer is implemented by an STM32F103C ARM-Cortex M3 microcontroller with clock speed up to 72 MHz.

The sampling rate of the CPU for each one of the eight 12 bit-ADC channels is set to 400 kHz. Since the output FIFO is 8-bit wide, every sample has to occupy 2 consequent bytes on the output pins. This means that the number of Kbyte/sec on the sampling layer output has to be 800 Kbyte/sec or 6.4 Mbit/sec, and the transfer of the Host has to be synchronized on 6.4 Mbit/sec for each channel. The total channel bandwidth on the next layer will have to be at least 51.2 Mbit/sec on the USB bus, since every byte has eight bit (Figure 8).

As layer 2 for Sampling and digitizing a development board from Olimex with an STM32F103C M3 Cortex onboard was used to collect the analog signals and output them on the 8-pin bus of the layer 3 FIFO. The layer 3 FTDI UM232H header board was soldered on the prototyping area of the STM23-106P board (Figure 9).

2.3. Layer 3: Transfer. The fast transfer of the acquired data to the host computer at speeds that exceed 50 Mbit/sec is

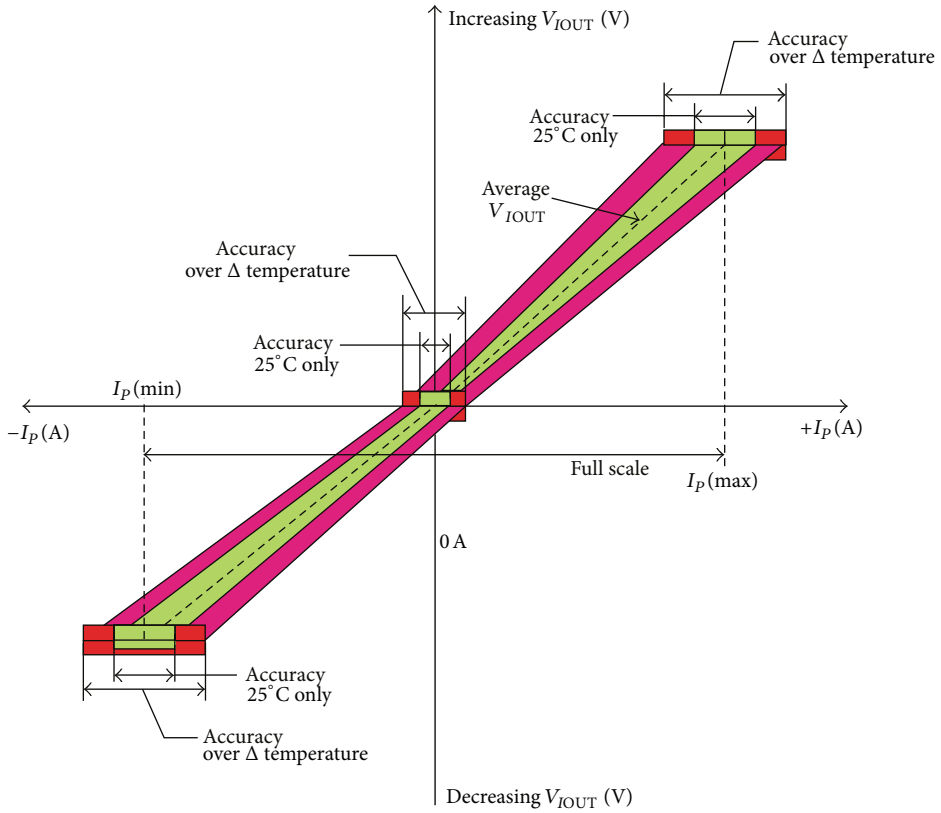

FIGURE 3: ACS712 output voltage versus sensed current. Accuracy at zero amperes and at full scale current [6].

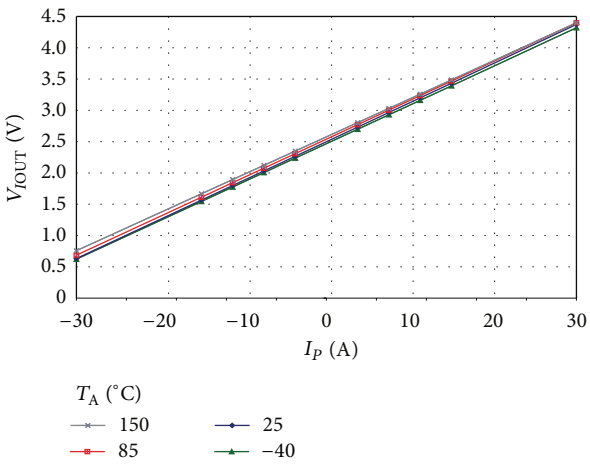

FIGURE 4: ACS712 output voltage versus sensed current for −10 A to 10 A range [6].

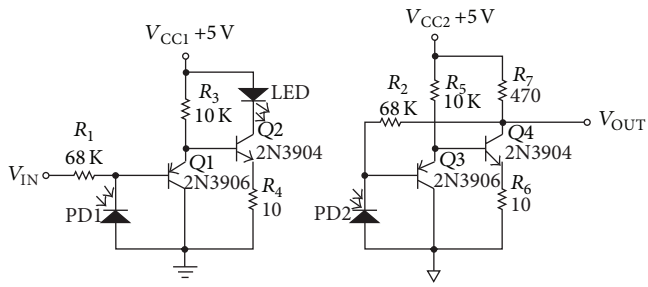

FIGURE 5: HCNR200 basic topology for voltage optoisolation. The voltage signal is prior limited to the appropriate levels by means of a preceding circuit with resistor dividers [7].

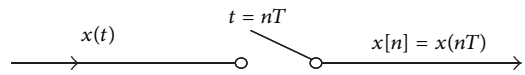

FIGURE 6: Sampling switch of analog signal and converting into discrete time sequence.

obtained thanks to UM232H, a single channel Hi-Speed USB development module by FTDI. This module utilizes the FT232H bridge IC which provides glue less and transparent transfer of data of the 8-bit parallel FIFO to the Host PC.

Below can be seen the main UM232H features [5].

(i) USB 2.0 Hi-Speed (480 Mbits/Second) and Full Speed (12 Mbits/Second) compatible.

(ii) Entire USB protocol handled on the chip—no USB-specific firmware programming required.

(iii) Small USB Type B connector common on many commercial devices.

(iv) USB bus or self-powered options.

(v) Support for USB suspend and resume.

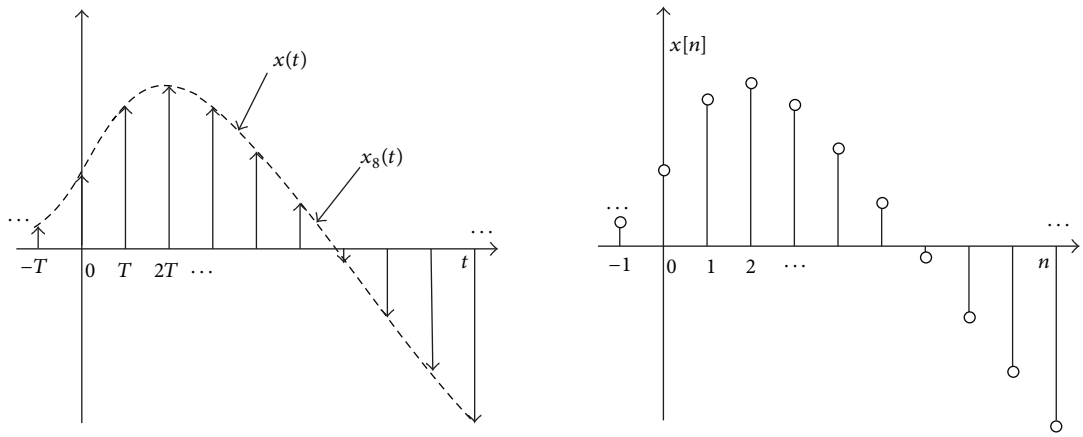

Figure 7: Converted analog signal into discrete time sequence diagrams.

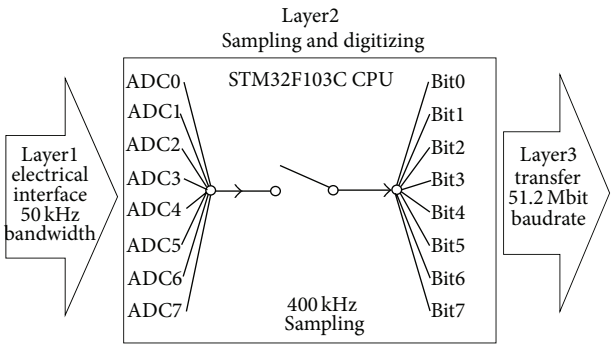

Figure 8: Sampling and digitizing schematic of Layer 2.

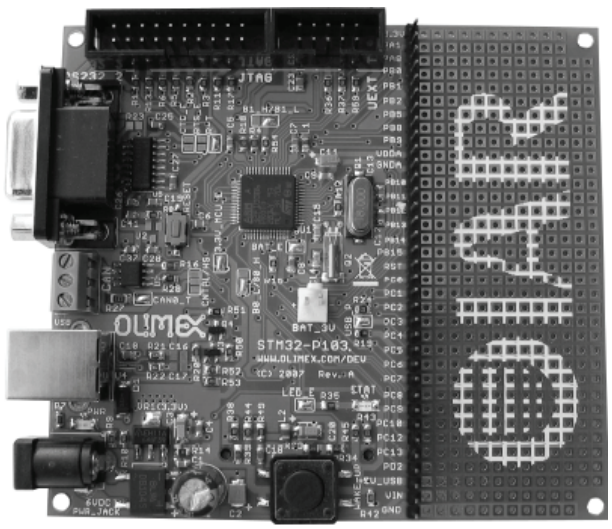

Figure 9: Olimex STM32-P106 with STM32F103C Prototyping Board used for sampling and digitizing.

(vi) UHCI/OHCI/EHCI host controller compatible.

(vii) FTDI's royalty-free VCP and D2XX drivers eliminate the requirement for USB driver development in most cases.

(viii) 1 kByte receive and transmit buffers for high data throughput.

(ix) Transmit and receive LED drive signals.

(x) Adjustable receive buffer timeout.

(xi) Synchronous and asynchronous bit bang mode interface options with RD# and WR# strobes.

(xii) Support for USB suspend and resume.

(xiii) Integrated 3.3 V level converter for USB I/O.

(xiv) USB bulk transfer mode.

(xv) +2.97 V to +5.25 V Single Supply Operation.

(xvi) Low operating and USB suspend current.

(xvii) Low USB bandwidth consumption.

(xviii) −40°C to + 85°C operating temperature range.

(xix) Rapid integration into existing systems.

FT232H can be configured in various modes of operation. For fast data transfer, the most convenient way is to configure the system in FT1248 mode [8]. In this mode the user CPU of layer 2 is the FT 1248 Master and the FT232H chip is the slave [4]. The protocol describes a synchronous transfer mode, where the synchronization signals are control from the Master. The transfer speed on the USB bus during this mode can reach up to 400 Mbit/sec (Figure 10).

The FT232H IC collects the data from Layer 2 in its 8-bit wide FIFO and then pumps the data automatically through the Hi-Speed USB 2.0 interface to the upper driver layer, the driver layer. The mode of operation and other configuration parameters are controlled via the driver and some special manufacturer software provided for free (Figure 11).

2.4. Layer 4: River. It is a fact that many electrical and power engineers working with electrical machines are familiar to embedded programming with microcontrollers for pulse generation, control and measurements. But when it comes to real time big data transfer to host computers, only a few non software engineers are able to complete this task. Usually

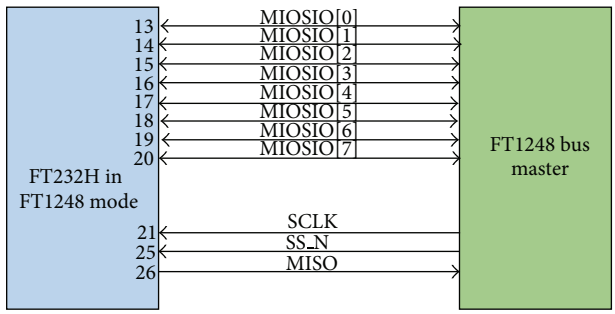

Figure 10: FT1248 Mode of operation master-slave connection signals [4].

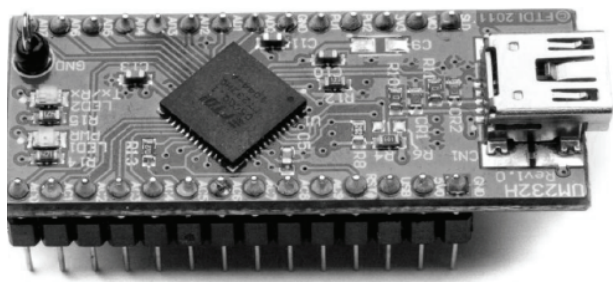

Figure 11: UM232H Parallel FIFO to Hi-Speed USB Module with FTDI FT232H chipset onboard.

people are connected to host computers with slower interfaces such as RS-232 and other protocols only for control and monitoring signaling. This happens because in order to send data through a fast interface such as USB, an intermediate piece of software needs to be written in privileged mode that accesses hardware resources directly and collects the data to be used by higher level applications. This software chunk is the driver that accompanies every USB device one can buy on the market. To be able to write USB drivers, professional software suites are necessary and a lot of practice (Figure 12).

On the other hand everyone can develop a high level application using high level programming languages such as C++, Java, Visual Basic, Python, and others. For this reason, the FT232H is provided with its driver ready and royalty-free by the manufacturer, along with a Dynamically Linked Library (DLL) file with which users can easily connect high level applications or a third party package such as MATLAB and LabView for further processing and presentation. This scheme is valid for Microsoft Windows operating systems but similar schemes exist for other popular OS such as Linux and MAC OS.

2.5. Layer 5: Application. The top layer of the proposed stack is the application Layer 5. This can be any high level software application written by the designer in any programming language one prefers, as long as he can access the D2XX DLL library functions provided by the manufacturer. Programmers and engineers can get from the FT232H IC manufacturer royalty free software examples for most popular

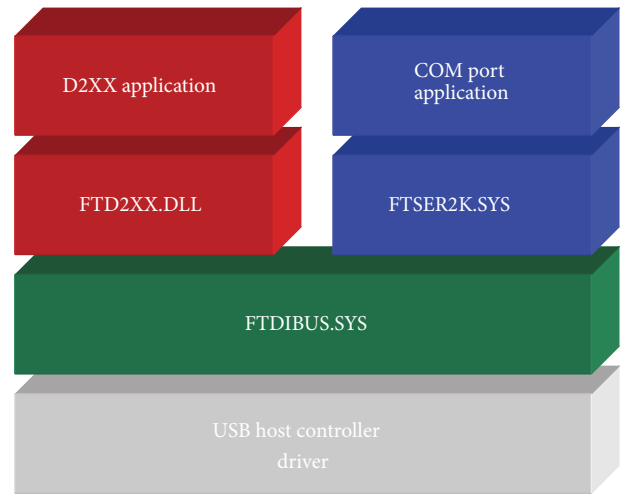

Figure 12: FTDI Driver stack for Microsoft Windows Operating System.

high level programming languages that demonstrate how to exchange data with the FT232H using the D2XX library.

In this work, the test implementation of the 5th Layer was done in MATLAB parsing the data directly from the D2XX library file receive buffer. When parsing data for all 8-channels the storage volume needed is 6.4 Mbyte/sec on the hard disk.

3. Conclusions

This paper presents an open architecture with very low cost and simple implementation for fast electrical machines voltage and current measurements in the laboratory. The main advantages of the proposed system are the replacement of expensive and big LEM hall effect transducers for current measurements with a low cost and very efficient hall effect transducer IC, the ACS712, as well as the use of a commercial low price hardware and software kit for the fast USB data transfer to a Host PC. The use of these two alternative solutions in measurement and transfer for signal sampling and the low design cost can be considered as original contribution of this work that could help many engineers to design their own measuring and sampling systems. The researcher or engineer will have to program no software for the transfer other than the usual microprocessor ADC parser and the top application layer data processing. The product is the UM232C Hi-Speed USB 2.0 to 8-bit parallel FIFO bridge module. The above described five layers' hardware and software stack for electrical machine measurements can be easily built in the laboratory and can replace expensive data acquisition cards and software that are widely used today.

In Tables 1 and 2 a short Billing of Material (BOM) analysis shows that the system can be built for about 112 USD in retail prices if ready development kits are used and around 59 USD if a special PCB board is designed to host the FT232H and STM32F103C ICs.

Table 1: Proposed measuring system architecture Billing of Material (BOM) for laboratory construction.

Item	Component	Qty	Value ($)
1	ACS712 Current Sensor	4	3.80
2	HCNR200 OptoIsolator	4	2.41
3	UM232H USB toFIFO Bridge	1	32.00
4	STM32-P106 Development Board	1	44.00
5	Other Components and Materials	1	3
6	Breakout Motherboard PCB	1	8
		Total	**111.84$**

Table 2: Proposed measuring system architecture Billing of Material (BOM) for laboratory construction without ready development modules including PCB design.

Item	Component	Qty	Value ($)
1	ACS712 Current Sensor	4	3.80
2	HCNR200 OptoIsolator	4	2.41
3	FT232H USB toFIFO Bridge IC	1	6.66
4	STM32F103C microprocessor	1	5.15
5	Other Components and Materials	1	10
6	Breakout Motherboard PCB	1	12
		Total	**58.65$**

If the implementation includes the PCB design to host the FT232H chip and the STM32F103C microprocessor on board without need to buy the ready development modules the cost is even lower as show in Table 2.

Although some initial tests for the proposed measurements system architecture were conducted in the laboratory, a lot has yet to be done to verify the system performance [1]. Some testing done included the sinusoidal and step input signals application produced by a frequency generator with variable frequency up to about 50 kHz where the limit of the ACS712 response was met. The jitter, error, and drift were found near the theoretically expected levels while further tests are to be done in order to verify the operation of the measurement platform. The next step will be to connect the system to a laboratory pair of electrical machines mechanically connected in common shaft. The pair consisted of a DC machine functioning as the prime mover and a three-phase synchronous machine that is the generator. The target is to measure all generator's terminal voltages and currents and compare them to measurements taken by another commercial measuring platform that will be used as golden unit.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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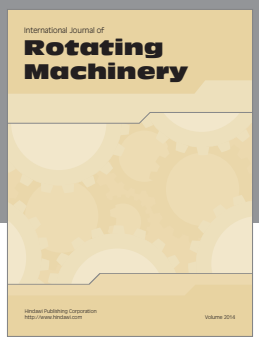

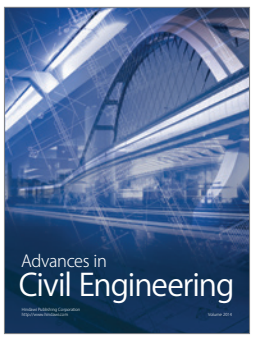

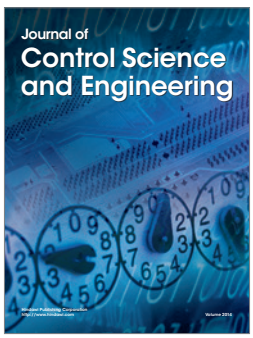

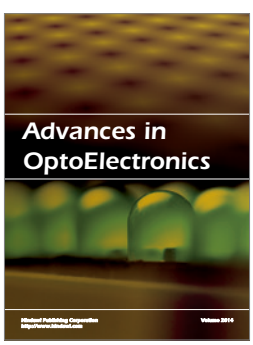

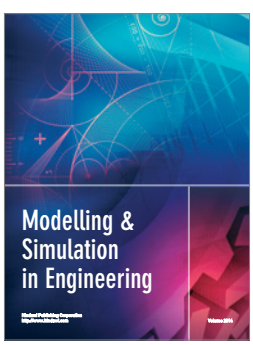

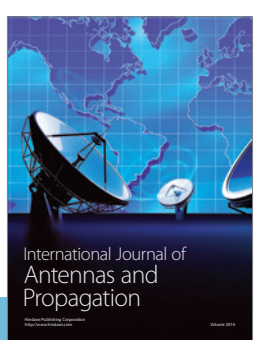

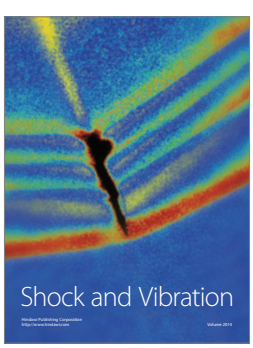

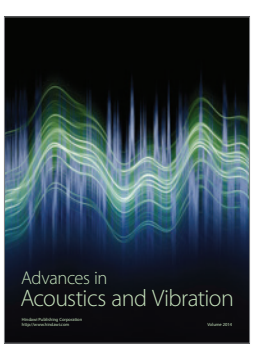

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